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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/990,935	LAM, WILLIAM	
	Examiner	Art Unit	
	Thomas H. Stevens	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11,13-21 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11,13-21 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 were examined.

2. Claims 2, 12 and 22 were cancelled.

3. Claims 1,3-11,13-21, 23-30.

Section I: Final Rejection (3rd Office Action)

Specification Objection

4. The disclosure is objected to because of the following informalities: reference application on page 16 is missing.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. Claims 1,3-6,8-11,13-16,18-21,23-26, 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable by Huang (U.S. Patent 5,095,454 (1992)) in view of Li (U.S. Patent 6,339,837 (2002)) and in further view of Casavant (U.S. 6,637,014 (2003)). Li teaches a method for verifying a digital circuit in a hardware description language using a verification structure and a verification engine; but doesn't teach critical paths or a single path after simulation or shortening the longest path. Huang teaches a digital simulation method and apparatus which provides a critical path for timing analysis of digital circuitry using a hybrid path tracing method; while Casavant teaches a method of shortening the critical path. At the time of invention, it would have been obvious to one of ordinary skill in the

art to modify Li by way of Huang and Casavant since the goal of static timing analysis is to complete a timing verification in a single pass (Huang: column 1, lines 60-61) with the ability to overcome delays related to crosstalk (Casavant: column 3, lines 45-47).

Claim 1. A method for amortizing a critical path computations (Huang: abstract) in a circuit comprising: unrolling (Li: column 5, lines 10-15) a data flow graph representing (Huang: column 4, lines 30-49) said circuit into a plurality of clock cycles (Huang: claim 15, lines 40-46); and simulating said circuit in said plurality clock cycles on a computer (Li: column 2, lines 23-30) wherein simulation further comprises reducing a difference between said critical path and a shortest path in said data flow graph (Casavant: column 4 ,lines 15-37).

Claim 3. The method of claim 1, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said step of reducing further comprises: compacting one or more computations from plurality of clock cycles in a processor.

Claim 4. The method of claim 1, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said step of unrolling further comprises: eliminating one or more flip-flops between (abstract: "eliminating

blocked paths") one or more boundaries (Huang: columns 8 and 9, lines 67-68, lines 1-2) within said plurality of clock cycles (Huang: claim 15, lines 40-46).

Claim 5. The method of claim 1, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said step of unrolling further comprise: eliminating one or more latches between (Huang: abstract: "eliminating blocked paths") one more boundaries (Huang: columns 8 and 9, lines 67-68, lines 1-2) within said plurality of clock cycles (Huang: claim 15, lines 40-46).

Claim 6. The method of claim 1, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said computer has a plurality of processors.

Claim 8. The method of claim 1, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said step of simulating further comprises: delaying evaluation of one or more logic elements (Huang: column 4, lines 42-46) within said plurality of clocks cycles (Huang: column 15, lines 40-46), thereby creating a timing slack (Huang: column 5, lines 25-30) for inter-processor communication (Li: column 7, lines 1-5).

Claim 9. The method of claim 1, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said step of reducing further comprises: using a first processor wherein said processor computes said critical path (Huang: column 14, lines 10-21) and a non-critical path in a said plurality of clock cycles (Huang: column 15, lines 40-46).

Claim 10. The method of claim 1, (Huang: abstract; claim 15, lines 40-46; Li: column 2, lines 23-30; Li: column 5, lines 10-15) further comprising: compacting said plurality of clock cycles into a single clock cycle (Huang: column 15, lines 55-60).

Claim 11. A critical path (Huang: column 14, lines 10-21) computation amortizer for a circuit comprising: a data flow graph (Huang: column 4, lines 30-49) unroller (Li: column 5, lines 10-15) configured to represent said circuit into a plurality of clock cycles (Huang: claim 15, lines 40-46); and a simulator configured to simulate said circuit in said plurality of clock cycles on a computer (Li: column 2, lines 23-30) wherein the simulator further comprise a reducer configured to reduce a difference between said critical path and a shortest path (Casavant: column 4, lines 15-37).

Claim 13. The critical path (Huang: abstract) computation amortizer of claim 11, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li:

column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said reducer further comprises: a compactor configured to compact one or more computations from said plurality of clock cycles in a processor.

Claim 14. The critical path (Huang: abstract) computation amortizer of claim 11, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said unroller further comprises: an eliminator configured to eliminate one or more flip-flops at one or more boundaries within said plurality of clock cycles.

Claim 15. The critical path computation amortizer of claim 11, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said unroller further comprises: an eliminator configured to eliminate one or more latches between (Huang: abstract: "eliminating blocked paths") one or more boundaries (Huang: columns 8 and 9, lines 67-68, lines 1-2) within said plurality of clock cycles (Huang: claim 15, lines 40-46).

Claim 16. The critical path (Huang: abstract) computation amortizer 11, (Huang: abstract; claim 15, lines 40-46; Li: column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said computer has a plurality of processors.

Claim 18. The critical path (Huang: abstract) computation amortizer of claim 11, (Huang: abstract; claim 15, lines 40-46; Li: column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said simulator is further configured delay evaluation of one or more logic elements (Huang: column 4, lines 42-46) in said plurality of clock cycles, (Huang: column 15, lines 40-46) thereby creating a timing slack (Huang: column 5, lines 25-30) for inter-processor communication (Li: column 7, lines 1-5).

Claim 19. The critical path (Huang: abstract) computation amortizer of claim 13, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said reducer further comprises: a feed-back configured to use a first processor wherein, said first processor computes said critical path (Huang: column 14, lines 10-21) and a non-critical path in said plurality of clock cycles (Huang: column 15, lines 40-46).

Claim 20. The critical path (Huang: column 14, lines 10-21) computation amortizer of claim 11, (Huang: column 14, lines 10-21; (Li: column 5, lines 10-15; Huang: claim 15, lines 40-46; Li: column 2, lines 23-30; Casavant: column 4, lines 15-37) further comprising: a scheduling compactor configured to compact said plurality of clock cycles into a single clock cycle (Huang: column 15, lines 55-60).

Claim 21. A computer program product comprising: a computer usable medium having computer readable code embodied therein configured to amortize a critical computation (Huang: abstract) in a circuit, said computer program product comprising: computer readable code configured to cause a computer to unroll (Li: column 5, lines 10-15 with figures 5 and 6) a data flow graph representing (Huang: column 4, lines 30-49) said circuit into a plurality of clock cycles; and computer readable code configured to cause a computer to simulate said circuit in said plurality of clock cycles on a computer (Li: column 2, lines 23-30) by at least causing the computer to reduce a difference between said critical path and a shortest path (Casavant: column 4, lines 15-37).

Claim 23. The computer program product of claim 21, (Huang: abstract; Li: column 5, lines 10-15 with figures 5 and 6; Li: column 2, lines 23-30; Huang: column 5, lines 45-55; Casavant: column 4, lines 15-37) wherein said computer readable code configured to cause a computer to unroll (Li: column 5, lines 10-15) further comprises: computer readable code configured to cause a computer to eliminate one or more flip-flops (abstract: "eliminating blocked paths") at one more boundaries within said plurality of clock cycles (Huang: claim 15, lines 40-46).

Claim 24 The computer program product of claim 21, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li:

column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said computer readable code configured to cause a computer to unroll further comprises (Li: column 5, lines 10-15): computer to eliminate one or more flip-flops (abstract: "eliminating blocked paths") at one or more boundaries within said plurality of clock cycles.

Claim 25. The computer program product of claim 21, (Huang: abstract; claim 15, lines 40-46; Huang: column 5, lines 45-55; Li: column 2, lines 23-30; Li: column 5, lines 10-15; Casavant: column 4, lines 15-37) wherein said computer readable code configured to cause a computer to unroll further comprises (Li: column 5, lines 10-15): computer readable code configured to cause a computer to eliminate one or more latches (Huang: abstract-- "eliminating blocked paths") at one or more boundaries within said plurality of clock cycles.

Claim 26. The computer program product of claim 21, (Huang: abstract; Li: column 5, lines 10-15 with figures 5 and 6; Li: column 2, lines 23-30; Casavant: column 4, lines 15-37) wherein said computer has a plurality of processors.

Claim 28. The computer program product of claim 21, (Huang: abstract; Li: column 5, lines 10-15 with figures 5 and 6; Li: column 2, lines 23-30) wherein said computer readable code configured to cause a computer to simulate comprises: computer readable code configured to cause a computer to delay evaluation (Huang: column 5, lines 25-31) of one or more logic elements in said

plurality of clock cycles (Huang: column 15, lines 40-46), thereby creating a timing (Huang: column 5, lines 25-31) slack for inter-processor communication.

Claim 29. The computer program product of claim 21, (Huang: column 14, lines 10-21; Huang: column 14, lines 10-21; (Li: column 5, lines 10-15; Huang: claim 15, lines 40-46; Li: column 2, lines 23-30; Huang: column 15, lines 55-60; Casavant: column 4, lines 15-37) wherein said computer readable code configured to cause a computer to reduce further comprises: computer readable code configured to cause a computer to use a first processor wherein said first processor computes said critical path (Huang: column 14, lines 10-21) and a non-critical path in said plurality of clock cycles(Huang: column 15, lines 40-46).

Claim 30. The computer program product of claim 21, (Huang: abstract; Li: column 5, lines 10-15 with figures 5 and 6; Li: column 2, lines 23-30; Casavant: column 4, lines 15-37) further comprising: computer readable code configured to cause a computer to compact said plurality of clock cycles (Huang: claim 15, lines 40-46) into a single clock cycles (Huang: column 15, lines 55-60).

7. Claims 7,17 and 27 are rejected under 35 U.S.C. 103(a) as being obvious by Huang (U.S. Patent 5,095,454 (1992)) in view of Abts et al., (U.S. Patent 6,856,950 (2005)) and in further view Li (U.S. Patent 6,339,837 (2002)). Li teaches a method for verifying a digital circuit in a hardware description language using a verification structure and a verification engine; but doesn't teach critical

paths or a single path after simulation or hardware support for barrier synchronization. Huang teaches a digital simulation method and apparatus which provides a critical path for timing analysis of digital circuitry using a hybrid path tracing method, while Abts et al., teaches a system and method of verifying an electronic system with the ability construct a interconnection network (Abts: column 49, lines 20-25) with hardware support for barrier synchronization (Abts: column 49, lines 25-31).

At the time of invention, it would have been obvious to one of ordinary skill in the art to modify Li by way of Huang and Abts et al., since the goal of static timing analysis is to complete a timing verification in a single pass (Huang: column 1, lines 60-61) and to have diagnostic system as well as a interprocess communication mechanism for transforming stimulus from the diagnostic system to the hardware simulation for transferring results from the hardware simulator to the diagnostic system (Abts: column 3, lines 2-5).

Clam 7. The method of claim1, (Huang: abstract; claim 15, lines 40-46; Li: column 2, lines 23-30; Li: column 5, lines 10-15) wherein said computer has a plurality of simulation processors, wherein said simulation processors include a communication network interconnecting (Li: column 7, lines 1-5) said simulation processors for data communication, (Li: column 7, lines 1-5) said simulation processors further including a synchronization network (Abts: column 49, lines 21-27) interconnecting said simulation processors for synchronizing execution (Abts: column 49, lines 21-27) there between.

Claim 17. The critical path computation amortizer of claim 11, (Huang: column 14, lines 10-21; Li: column 5, lines 10-15; Huang: claim 15, lines 40-46; Li: column 2, lines 23-30) wherein said computer has a plurality of simulation processors, wherein said simulation processors include a communication network interconnecting (Li: column 7, lines 1-5) said simulation processors for data communication, (Li: column 7, lines 1-5) said simulation processors further including a synchronization network (Abts: column 49, lines 21-27) interconnecting said simulation processors for synchronization execution (Abts: column 49, lines 21-27) there between.

Claim 27. The computer program product of claim 21, (Huang: abstract; Li: column 5, lines 10-15 with figures 5 and 6; Li: column 2, lines 23-30) wherein said computer has a plurality of simulation processors, wherein said simulation processors include a communication network (Li: column 7, lines 1-5) interconnecting said simulation processors for data communication, said simulation processors further including a synchronization network (Abts: column 49, lines 21-27) interconnecting said simulation processors for synchronizing execution (Abts: column 49, lines 21-27) there between.

Section II: Response to Applicants Arguments

112 1s and 2nd

6. Applicants are thanked for addressing this issue. Rejections are withdrawn.

103

7. Applicants are thanked for addressing this issue. Based on an updated search, the Office has found new art based on the amended claims; however, the 103 rejection from the previous office action is withdrawn.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Leo Picard at (571) 272-3749. Central Fax number is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

August 30, 2005

Paul L. Rodriguez 8/31/05

Primary Examiner
Art Unit 2125

THS